Applicants' claimed invention pertains to a method of fabricating a self-aligned contact (FIG. 9B or FIG. 16) in which a contact plug 44 connects a conductive region 31 formed at the top of a semiconductor substrate 30 to a conductive line 34 or 34'. According to one aspect of the present invention, the contact plug 44 penetrates the conductive line 34 or 34'.

To this end, independent claim 1 calls for, in part, steps of forming the conductive line 34 on an interlayer dielectric layer 32 (FIG. 3A), **removing portions of the conductive line 34 to form a contact hole 42** that exposes the conductive region 31 (FIG.7B), and filling the contact hole 42 with conductive material (FIG. 9A). Alternatively, independent claim 9 calls for steps of forming a **conductive line 34' having a gap** on an interlayer dielectric layer 32 (FIG. 1), removing a portion of the interlayer dielectric layer 32 to form a contact hole 42 that exposes the conductive region 31 (FIG. 15) via the gap, and filling the contact hole 42 with conductive material (FIG. 16).

In contrast, the Jeng reference, the contact plug 28 does not penetrate the conductive line 32 since the conductive plug 28 is formed prior to forming the conductive (bit) line 32. Thus, the method disclosed by Jeng is no different from Applicants' admitted prior art of FIGS. 1 and 2, in this respect. (See Applicants' original specification, page 19, lines 23-29).

More specifically, Jeng et al. do disclose a method of fabricating a self-aligned contact in which a contact plug 28 connects a conductive region 17 formed at the top of

a semiconductor substrate 10 to a conductive bit line 32 (FIGS. 11 and 12). However, the steps used in fabricating this structure can not be read on Applicants' method of claims 1 or 9. To illustrate this point, claims 1 and 9 have been reproduced below with the most appropriate reference numerals from the Jeng et al. reference inserted therein. The main differences between Applicants' method claims 1 and 9 and the method disclosed by Jeng et al. are made apparent by way of underlining and bracketing.

1. A method of fabricating a semiconductor device, comprising:

forming a conductive region (17) at the top of a semiconductor substrate (10);

forming a first interlayer dielectric layer (20) on the semiconductor substrate over the entirety of the conductive region (17);

forming a conductive line (32), which is to be connected to the conductive region (17), on the first interlayer dielectric layer (20);

forming a second interlayer dielectric layer (34) on the conductive line (32);

removing portions of the first interlayer dielectric layer 20 only [, conductive line (32), and second interlayer dielectric layer (34) which overlie the conductive region (17)] to form a contact hole (FIG. 7 ➜ FIG. 8) which exposes the conductive region (17); and

filling the contact hole with a conductive material (28) to connect the conductive line to the conductive region.

9. A method of fabricating semiconductor devices, comprising:

forming a conductive region (17) at the top of a semiconductor substrate (10);

forming a first interlayer dielectric layer (20) on the semiconductor substrate over (10) over the entirety of the conductive region (17);

forming a conductive line (32), which is to be connected to the conductive region (17), on the first interlayer dielectric layer (20), [the conductive line having a gap therein of a predetermined width];

forming a second interlayer dielectric layer (34) on the conductive line (32) [such that a first portion of the second interlayer dielectric layer occupies the gap in the conductive line (32)];

removing a portion of the first interlayer dielectric layer (20) overlying the conductive region (17) only [, the first portion of the second interlayer dielectric layer (34) occupying the gap in the conductive line (32), and a second portion of the second interlayer dielectric layer (34) overlying the gap] to form a contact hole (FIG. 7 ➜ FIG. 8); and

filling the contact hole with a conductive material to connect the conductive line (32) to the conductive region (17).

In the method of Jeng et al., only portions of the first dielectric layer 20 are removed to form the contact hole, seeing the contact plug 28 is formed before the conductive bit line 32 and overlying dielectric layer 34 are formed. On the other hand,

concerning claim 1, portions of the conductive line and second dielectric layer formed on the conductive line are removed, to form the contact hole; the contact plug is formed after the conductive line is formed so that it can penetrate the conductive line.

In other words, referring to FIGS. 5-9 of the Jeng et al. reference, a shallow trench (25A) is formed by etching the dielectric layer (20) corresponding to the first interlayer dielectric layer of the present claims, using polysilicon pattern (22), to form a polysilicon spacer (26) on the sidewalls of the polysilicon pattern. Then, self-aligned etching is carried on the dielectric layer (20) using the polysilicon pattern (22) and the polysilicon spacer (26) to form a contact hole, which is then filled with polysilicon to form a plug (28). Then, a dielectric layer (30) corresponding to the second interlayer dielectric layer of the present claims is formed and patterned, as shown in FIG. 10. Then, another contact hole is formed only in dielectric layer (30) and polyside layer (32) corresponding to the conductive line of the present claims is thereafter deposited to occupy this another contact hole, as shown in FIG. 11 of the Jeng et al. reference. In contrast, in the present invention and in claim 1 particularly, the first interlayer dielectric layer, the conductive line and the second interlayer dielectric layer are removed to form a contact hole that exposes the conductive region. In the Jeng et al. reference, only dielectric layer (20) is removed to expose the conductive region in the substrate.

Concerning claim 9, there is no disclosure in the Jeng et al. reference corresponding to the several limitations in claim 9 pertaining to the gap in the conductive line 34' (FIG. 11) that is filled with conductive material to form the conductive

plug, whereby the contact plug penetrates the conductive line.

With regard to claim 2, although Jeng et al. disclose forming a patterned photosensitive film on the second dielectric layer 34 formed on conductive line 32 (col. 5, lines 30-37), the openings in such a film are not disclosed as having a width greater than the CD of the conductive line 32 nor is the film used in a process for etching away a portion of the conductive line 32. In addition, the polysilicon hard masks referred to by the Examiner are only used for etching the first dielectric layer 20 formed on the semiconductor substrate 10 over the conductive region 17. Thus, the Jeng et al. reference does not anticipate claim 2 or any of claims 3-7 depending from claim 2.

Similarly, as concerns claim 10, seeing that there is no disclosure in Jeng et al. of the conductive line 32 having a gap therein, there is no disclosure in Jeng et al. of forming a patterned photosensitive film on the second dielectric layer 34, and which film defines an opening having widths (See Applicants' FIG. 12) in two orthogonal directions that are greater than the CD of and the width of a gap in the conductive line. It also follows that Jeng et al. do not disclose anything corresponding to the claimed step of etching dielectric that occupies the gap in a conductive line. Thus, the Jeng et al. reference does not anticipate claim 10 or any of the claims depending therefrom.

For the foregoing reasons, namely because of the differences between Applicants' claimed invention and the prior art, including the lack of disclosure in Jeng et al. of a method of fabricating a contact in which the contact hole is formed through the conductive line, the reference does not anticipate Applicants' claims under 35 USC 102. Accordingly, early reconsideration and allowance of the claims are respectfully requested.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

for Michael Stone
Registration No. 32,442 Reg # 33,581

12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Date: November 14, 2001

Enclosures: Version with marked-up changes

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Abstract

A semiconductor device includes a conductive region[, a conductive] and line, and a contact plug electrically connecting the [conductive] line and [to] the [conductive] region. The [conductive] line is [electrically] connected to the [conductive] region via [the] sidewalls of the [contact] plug, and the [conductive] region is [electrically] connected to the [conductive] line via the bottom of the [contact] plug. The cross-sectional area of the [contact] plug decreases in a direction from [the] an upper to lower portion [of the contact plug to the lower portion] thereof. In a first method of fabricating a semiconductor device having a self-aligned contact, the [contact] plug is formed after the [conductive line is formed. In a first method, a conductive] line is formed in an interlayer dielectric layer. Portions of the [interlayer] dielectric layer and [conductive] line are etched to form a contact hole in which the [contact] plug is formed. In a second method, a [conductive] line having a gap therein is formed in an interlayer dielectric layer. Portions of the [interlayer] dielectric layer, including [that occupying] the gap in the [conductive] line, are etched to form the contact hole.

Additions/Deletions to the Specification

***Page 2, lines 7-12*:**

When the contact plug 16, which is an underlying film pattern, and the conductive line 18, which is an overlying film pattern, are not accurately aligned, the operating characteristics of the resultant semiconductor device [is] are adversely

affected. Specifically, a reduction in the contact area between the contact plug 16 and the conductive line 18 increases the contact resistance, thereby reducing the operating speed of the semiconductor device.

Page 6, lines 1-9

Next, referring to FIGS. 4A and 4B, a second interlayer dielectric layer 36 is formed on the entire surface of the semiconductor substrate 30 on which the conductive line 34 has been formed. The second interlayer dielectric layer 36 may be a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a USG layer, a BSG layer, a BPSG layer, a PE-TEOS layer, a TEOS layer or an O_3-TEOS layer. If the upper surface of the second interlayer dielectric layer 36 is not flat, the entire surface thereof can be planarized by [an] a method appropriate to the material thereof, e.g., a chemical mechanical polishing (CMP) method, an etch back method, or a thermal reflow method.

Page 7, lines 10-17

The etching of the second interlayer dielectric layer 36 preferably stops at the upper surface of the conductive line 34. In this case, the portions 40 of the second interlayer dielectric layer on the left and right sides of the conductive line 34 are exposed, as shown in FIG. 5A, because the first width W_1 is larger than the critical dimension D of the conductive line 34. For reasons that will be described in more detail later on, in the first embodiment of the present invention, the finally formed self-aligned contact is to have [the] a width no smaller than the critical dimension D of the

conductive line 34.

Page 10, lines 3-22

Referring to FIGS. 9A and 9B, a [conducive] conductive material is deposited in the contact hole 42 and on the second interlayer dielectric layer 36 to form a conductive layer. Here, the inclined sidewalls of the second interlayer dielectric layer 36 provide an improved step coverage of the conductive layer and prevent defects, such as voids, from occurring. Subsequently, the upper surface of the semiconductor substrate on which the conductive layer has been formed is planarized by CMP or an etch back method. The conductive layer can be an aluminum layer, a copper layer, a gold layer, a silver layer, an impurity-doped polysilicon layer, a tungsten layer, a platinum layer, a tungsten silicide layer, a titanium silicide layer or a combination of the above-mentioned layers. Preferably, the planarization stops when the upper surface of the conductive line 34 is reached. The contact plug 44 connecting the conductive line 34 to the conductive region 31 is formed once the upper surface of the conductive line 34 is exposed by the planarization process. The contact plug 44 is thus a self-aligned contact formed between the conductive line 34 and the conductive region 31. Note, before the conductive layer is formed, a barrier metal layer (not shown) may be formed to improve the adhesiveness between the contact plug 44 and the first interlayer dielectric layer 32 and prevent the material constituting the contact plug 44 from being diffused into the first interlayer dielectric layer 32. The barrier metal layer may be a Ti/TiN film. However, the barrier metal layer is not limited to being a Ti/TiN film.

Additions/Deletions to the Claims

14. (Amended) The method of claim [11] 21, further comprising removing the photosensitive film pattern after the portion of the conductive line defining the gap therein is exposed.